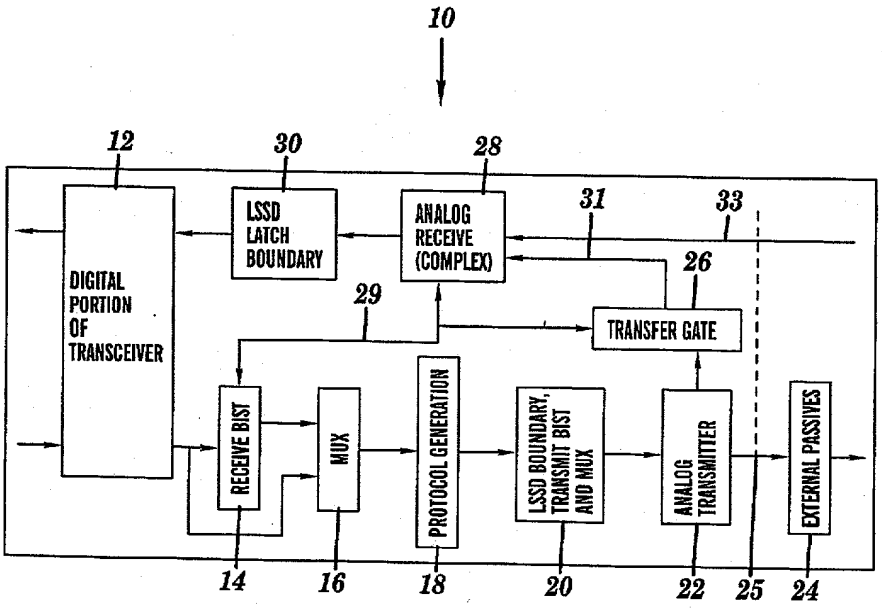

10
12
30
28
31
33
26
29
DIGITAL PORTION OF TRANSCEIVER
LSSD LATCH BOUNDARY
ANALOG RECEIVE (COMPLEX)
TRANSFER GATE
RECEIVE BIST
MUX
PROTOCOL GENERATION
LSSD BOUNDARY, TRANSMIT BIST AND MUX
ANALOG TRANSMITTER
EXTERNAL PASSIVES
14
16
18
20
22
25
24

FIG. 1

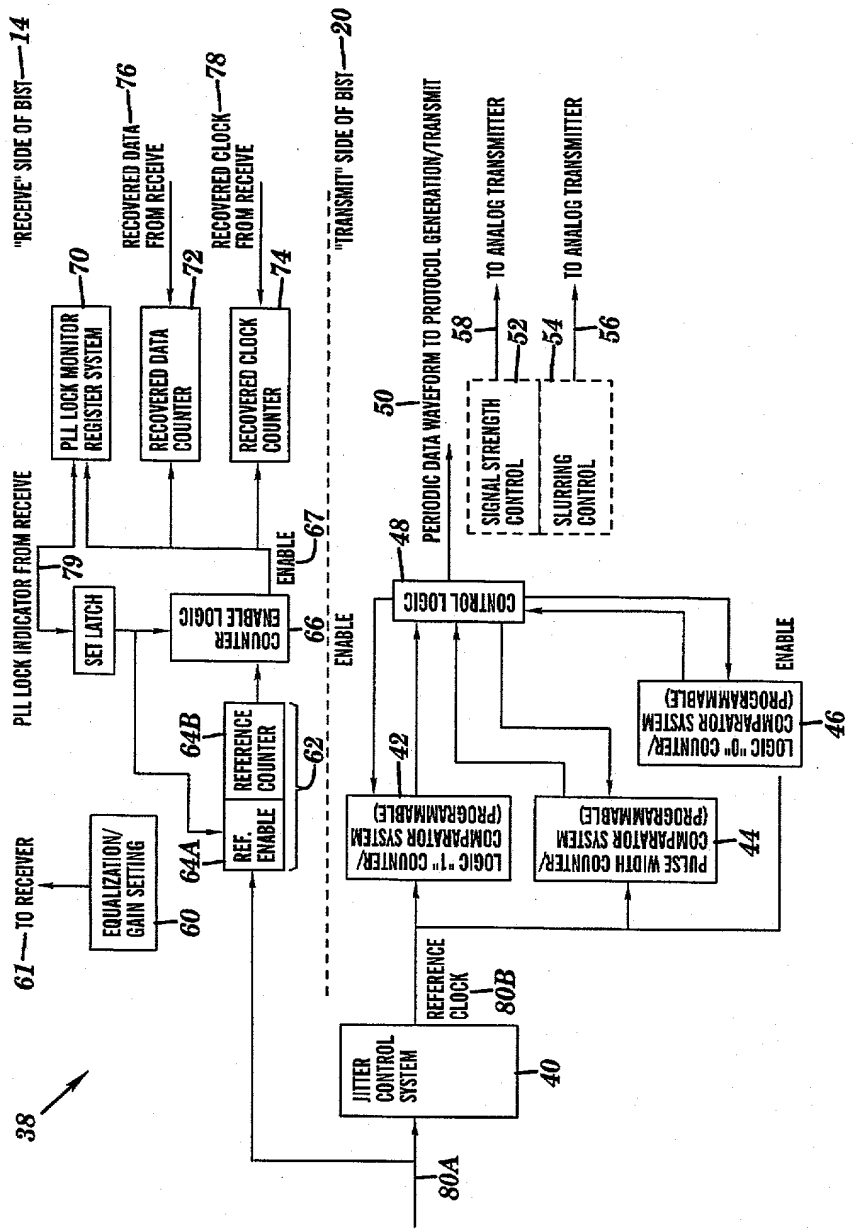

"RECEIVE" SIDE OF BIST
14
"TRANSMIT" SIDE OF BIST
20
PLL LOCK INDICATOR FROM RECEIVE
79
PLL LOCK MONITOR REGISTER SYSTEM
70
RECOVERED DATA FROM RECEIVE
76
RECOVERED DATA COUNTER
72
RECOVERED CLOCK FROM RECEIVE
78
RECOVERED CLOCK COUNTER
74
SET LATCH
COUNTER ENABLE LOGIC
66
ENABLE
67
ENABLE
REFERENCE COUNTER
62
64B
REF. ENABLE
64A
EQUALIZATION/ GAIN SETTING
60
61
TO RECEIVER
38
CONTROL LOGIC
48
PERIODIC DATA WAVEFORM TO PROTOCOL GENERATION/TRANSMIT
50
SIGNAL STRENGTH CONTROL
52
58
TO ANALOG TRANSMITTER
SLURRING CONTROL
54
56
TO ANALOG TRANSMITTER
LOGIC "1" COUNTER/ COMPARATOR SYSTEM (PROGRAMMABLE)
42
PULSE WIDTH COUNTER/ COMPARATOR SYSTEM (PROGRAMMABLE)
44
LOGIC "0" COUNTER/ COMPARATOR SYSTEM (PROGRAMMABLE)
46
ENABLE
REFERENCE CLOCK
80B
JITTER CONTROL SYSTEM
40
80A

FIG. 2

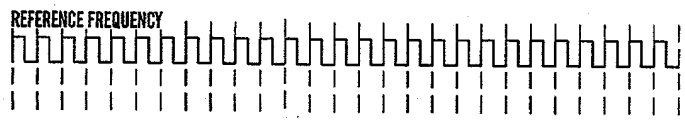


FIG. 3A

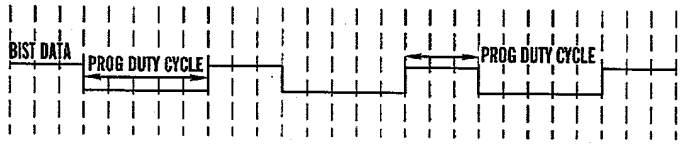


FIG. 3B

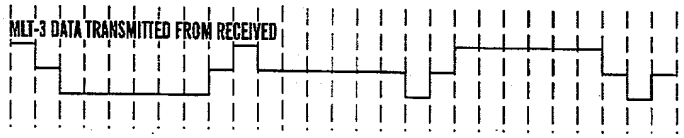


FIG. 3C

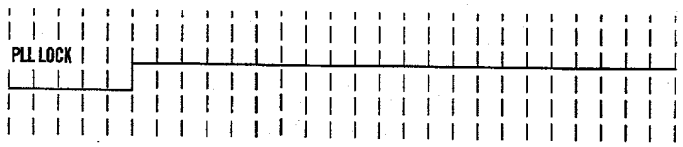


FIG. 3D

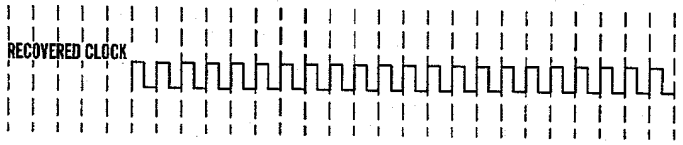


FIG. 3E

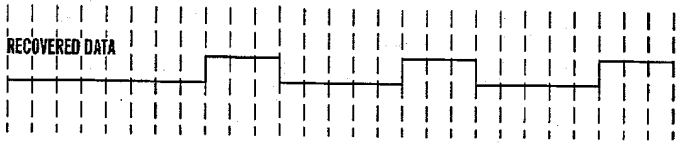


FIG. 3F

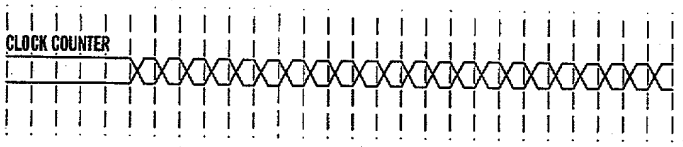


FIG. 3G

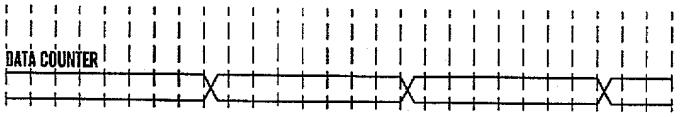


FIG. 3H

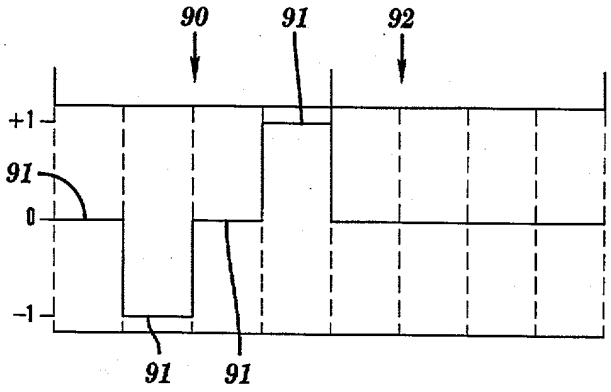


FIG. 4A

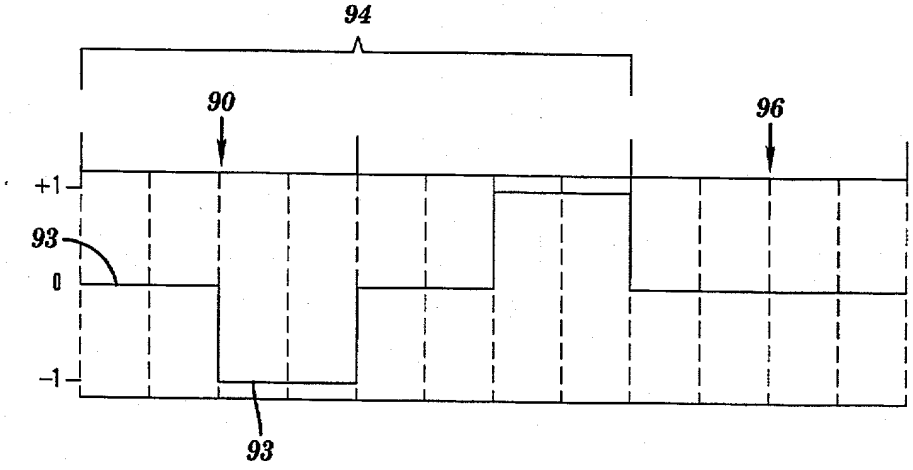


FIG. 4B

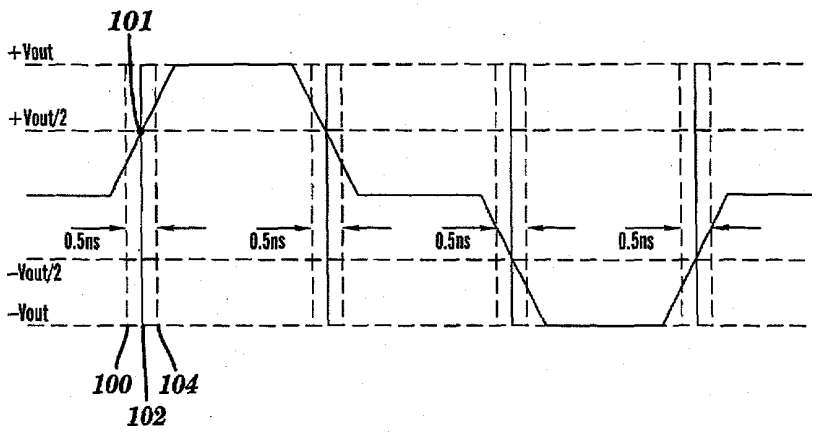


FIG. 5

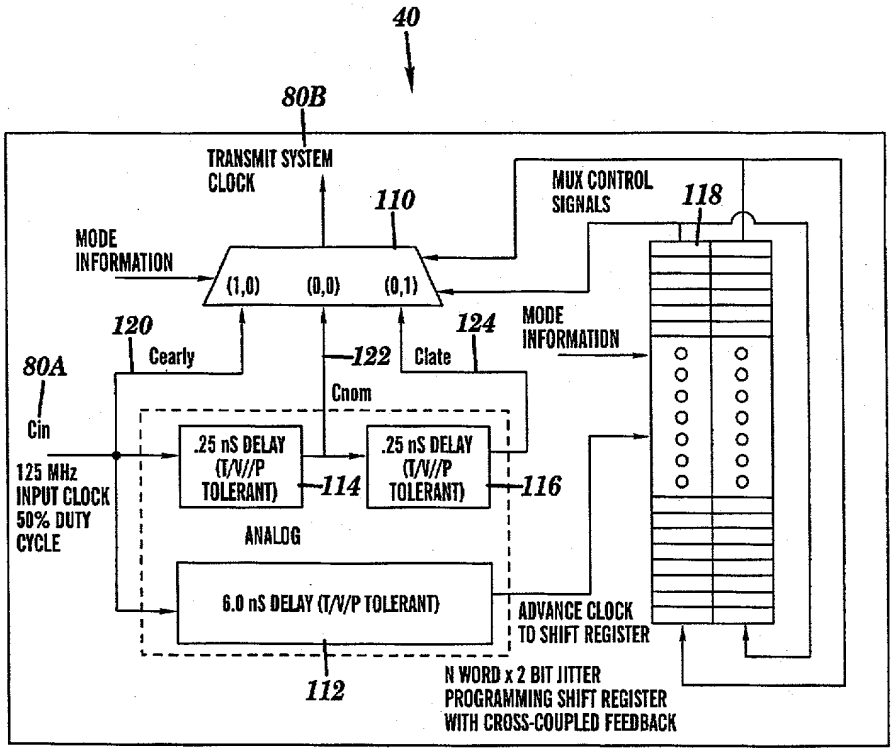

40
80B
TRANSMIT SYSTEM CLOCK
110
MUX CONTROL SIGNALS
118
MODE INFORMATION
(1,0)
(0,0)
(0,1)
120
Cearly
122
Clate
124
MODE INFORMATION
80A
Cnom
Cin
125 MHz INPUT CLOCK 50% DUTY CYCLE
.25 nS DELAY (T/V//P TOLERANT)
114
.25 nS DELAY (T/V//P TOLERANT)
116
ANALOG
6.0 nS DELAY (T/V/P TOLERANT)
ADVANCE CLOCK TO SHIFT REGISTER
112
N WORD x 2 BIT JITTER PROGRAMMING SHIFT REGISTER WITH CROSS-COUPLED FEEDBACK

FIG. 6

FIG. 7A

FIG. 7B

FIG. 7C

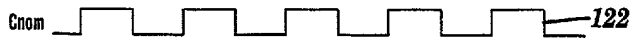


FIG. 7D

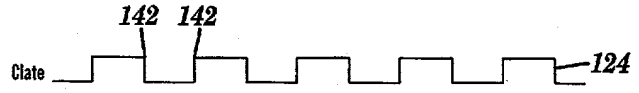


FIG. 7E

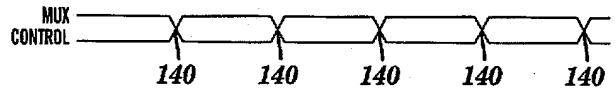
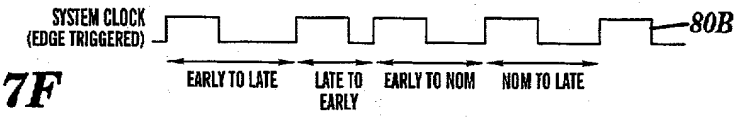


FIG. 7F



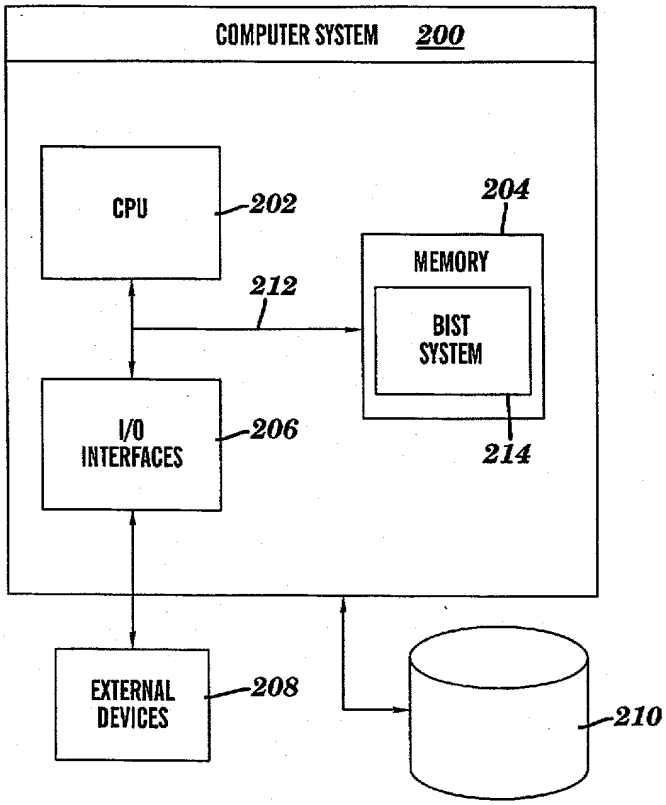

COMPUTER SYSTEM 200
CPU
202
204
MEMORY
212
BIST SYSTEM
I/O INTERFACES
206
214
EXTERNAL DEVICES
208
210

FIG. 8